IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF FOR THE APPELLANTS

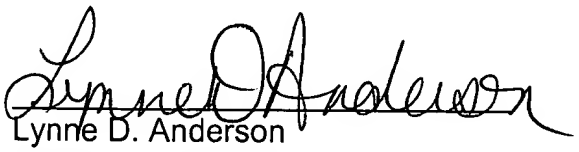
Ex parte Takeno

MANUFACTURING PROCESS FOR SILICON EPITAXIAL WAFER

Serial Number: 09/926,202
Filed: September 24, 2001
Appeal No.:
Group Art Unit: 1765
Examiner: M. Anderson

A check in the amount of Three Hundred Thirty Dollars ($330.00) is enclosed to cover the official fees for this Appeal Brief and a Petition for One Month Extension of Time ($110.00). Please charge any fee deficiencies required with respect to this paper, or overpayment to our Deposit Account No. 01-2300, **referencing docket number 107242-00024**.

Respectfully submitted,



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In re the Application of:

Takeno

Application No.: 09/926,202

Filed: September 24, 2001

Art Unit: 1765

Examiner: M. Anderson

Attorney Dkt. No.: 107242-00024

For: MANUFACTURING PROCESS FOR SILICON EPITAXIAL WAFER

BRIEF ON APPEAL

I. INTRODUCTION

This is an appeal from the action of the Examiner dated September 10, 2003, finally rejecting claims 6-21 as being unpatentable over certain prior art under 35 U.S.C. §103. A Notice of Appeal was timely filed on December 8, 2003.

II. REAL PARTY IN INTEREST

The real party in the interest in present application on appeal is SHIN-ETSU HANDO-TAI, CO., LTD 4-2 MARUNOUCHI 1-CHOME, CHIYODA-KU, TOKYO, JAPAN, by virtue of an Assignment recorded in the U.S. Patent and Trademark Office on September 24, 2001 at Reel 012341, Frame 0239.

III. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellants, Appellant's representative or Assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

IV. STATUS OF CLAIMS

Claims 6-21 are being appealed. Claim 6 is independent. Claims 7-21 depend directly or indirectly from claim 6. Claims 1-5 are cancelled. The claims on appeal are set forth in the attached Appendix I.

V. STATUS OF AMENDMENTS

All Amendments have been entered.

VI. SUMMARY OF THE INVENTION

A. Summary

The present invention to provides a process of manufacturing an epitaxial wafer having an internal gettering (IG) ability, wherein heat treatment is applied at a temperature in a range of from 450°C to 750°C to an epitaxial wafer in which oxygen precipitation nuclei are reduced in an epitaxial growth step so as to form new oxygen precipitation nuclei therein. Oxygen precipitation proceeds in a device fabrication process subsequent to the heat treatment, especially the oxide precipitates are effectively increased even when a wafer with a comparatively low oxygen concentration is used as a silicon substrate. (See page 4, lines 5-15 of the present specification)

B. The Claimed Invention

Claim 6 recites a manufacturing process for a silicon epitaxial wafer. The process includes the step of forming an epitaxial layer on a silicon substrate with an interstitial oxygen concentration in a range of from 4 x $10^{17}/cm^3$ to 10 x $10^{17}/cm^3$ at a

temperature of 1000° C or higher to obtain a silicon epitaxial wafer. The method also includes applying heat treatment to the silicon epitaxial wafer at a temperature in a range of from 450° C to 750° C, thereby forming new oxygen precipitation nuclei and increasing bulk defect density, without reducing internal gettering.

VII. THE FINAL REJECTION

Claims 6-21 are pending in this application. Claims 6-21 are finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Wijaranakula (U.S. Patent No. 5, 611, 855) in view of Wolf et al., *Silicon Processing* for the VLSI Era (Wolf).

VIII. ISSUES ON APPEAL

The issues on appeal are as follows:

(1) Whether there is proper motivation to combine Wijaranakula and Wolf to arrive at the claimed invention.

(2) Whether the oxygen concentration range and the epitaxial wafer heat treatment range are merely optimized process parameters.

(3) Whether there is any disclosure or suggestion in Wijaranakula, as modified by Wolf, to vary the substrate resistivity of the epitaxial wafer.

IX. GROUPING OF CLAIMS

Each claim of this patent application is separately patentable, and upon issuance of a patent, will be entitled to a separate presumption of validity under 35 U.S.C. § 282. For convenience in the handling of this appeal, the claims are grouped as follows:

Group I, independent claim 6 and dependent claims 14-21.

Group II, dependent claims 10-13.

Each of the Groups I-II will be argued separately in the following arguments. The Groups do not stand or fall together.

X. APPELLANT'S ARGUMENTS

The Law

In order to be unpatentable under 35 U.S.C. § 103, several basic factual inquiries must be made to determine obviousness or non-obviousness of the patent application claims. These factual inquiries are set forth in Graham v. John Deere Co., 383 U.S. 1,17,148 U.S.P.Q. 459, 467 (1996):

> Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; the level of ordinary skill in the pertinent art resolved. Against this backdrop, the obviousness or non-obviousness of the subject matter is determined.

Also, as stated by the Federal Circuit in In re Ochiai, 37 U.S.P.Q. 2d 1127, 1131 (Fed. Cir. 1995):

> [t]he test of obviousness vel non is statutory. It requires that one compare the claim's subject matter as a whole with a prior art to which the subject matter pertains. 35 U.S.C. § 103.
>
> The inquiry is highly fact-specific by design.... When the references cited by the Examiner fail to establish a prima facie case of obviousness, the rejection is improper and will be overturned. In re Fine, 837 F.2d 1071, 1074, 5 U.S.P.Q. 2d 1596, 1598 (Fed. Cir. 1988). (Emphasis added.)

When rejecting claims under 35 U.S.C. § 103, an Examiner bears an initial burden of presenting a prima facie case of obviousness. A prima facie case of

obviousness is established only if the teachings of the prior art would have suggested the claimed subject matter to a person of ordinary skill in the art. If an Examiner fails to establish a prima facie case, the rejection is improper and will be overturned. See: In re Rijckaert, 9 F.3d 1531, 28 U.S.P.Q. 2d. 1955 (Fed. Cir. 1993). "If examination... does not produce a prima facie case of unpatentability, then without more the applicant is entitled to the grant of the patent." In re Oetiker, 977 F.2d 1443, 1445-1446 24 U.S.P.Q. 2d. 1443, 1444 (Fed. Cir. 1992).

A. REJECTION OF CLAIMS 6-21 UNDER 35 U.S.C. § 103(a)

Claims 6-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wijaranakula (U.S. Patent No. 5,611,855) in view of Wolf et al. *Silicon Processing for the VLSI Era* (Wolf). In making this rejection, the final Office Action takes the position that Wijaranakula discloses all the elements of the claimed invention, except for disclosing the deposition temperature of the epitaxial layer or the oxygen concentration in units of atoms/cm^3. Wolf is cited for teaching these limitations. Appellant respectfully submits that claims 6-21 recite subject matter that is neither disclosed nor suggested in any combination of Wijaranakula or Wolf.

The final Office Action takes the position that the combination of Wijaranakula and Wolf discloses all of the elements of the claimed invention. However, it is respectfully submitted that the prior art fails to disclose or suggest the claimed invention, and therefore, fails to provide the advantages of the present invention. For example, as a result of the claimed invention, the manufacturing process of the present invention is configured such that heat treatment is applied at a temperature in a range of 450°C to

750°C to an epitaxial wafer in which oxygen precipitation nuclei are reduced in an epitaxial growth step so as to form new oxygen precipitation nuclei therein.

As a result of this, oxygen precipitation proceeds in the device fabrication process subsequent to the heat treatment. Thus, the oxide precipitates are effectively increased, even when a wafer with a comparatively low oxygen concentration is used as a silicon substrate.

1. Summary of Wijaranakula

Wijaranakula discloses a semiconductor silicon wafer and a method for manufacturing a calibration wafer having a microdefect-free layer of a precisely predetermined depth. The silicon wafer is formed by depositing an epitaxial layer onto a substrate having an interstitial oxygen concentration suitable for precipitating oxide. As shown in Figures 1-3, the semiconductor silicon wafer 10 comprises a semiconductor silicon substrate 12 that contains multiple oxide microdefects 14 and a microdefect-free layer 16 having a precise thickness 18 and extending from a front surface 20 of a semiconductor silicon wafer 10. The semiconductor silicon substrate 12 can be either intrinsic (having the conductivity of pure silicon) or extrinsic (having its conductivity changed by an added dopant such as boron, phosphorus, antimony, carbon or arsenic). The concentration of the added dopant is preferably less than 300 ppma.

Fig. 4 of the reference illustrates the method of producing the wafer shown in Figs. 1-3. Process step 42 indicates that an ingot of single crystal is grown. The specification states that it is grown using a Czochralski process. The growth process is such as to ensure that the resulting crystal ingot contains sufficient dissolved oxygen. The amount of dissolved oxygen is typically between 10 ppma and 50 ppma for forming

microdefects 14. In process step 44, the ingot is sliced into semiconductor silicon wafers and polished. The polished wafer forms a semiconductor silicon substrate 12 ready for process step 46, which entails depositing an epitaxial layer preferably by chemical vapor deposition. The epitaxial layer contains no sites or nuclei to form oxide microdefects during subsequent annealing steps and, therefore, provides a layer free of microdefects. Process step 48 shows that the semiconductor silicon substrate 12, along with the deposited epitaxial layer, is annealed at a temperature suitable to nucleate oxide microdefects. The temperature is preferably between 600°C and 900°C. Process step 50 shows that the semiconductor silicon substrate 12, along with the deposited defect free epitaxial layer, is annealed at a temperature to grow the oxide microdefects 14 that were nucleated in step 48 in the substrate 12.

2. Summary of Wolf

Wolf discloses specifications for silicon wafers for VLSI manufacturing.

Final Rejection

The final Office Action dated September 10, 2003 takes the position that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wijaranakula with the teachings of Wolf because Wolf discloses temperatures for epitaxial growth and annealing, oxygen concentrations, a basis for comparing oxygen concentrations quoted in different units resistivity of boron and antimony-doped Si, and the known useful gettering action of oxygen precipitates in Si Wafers.

The final Office Action further asserts that it also would have been obvious to one of ordinary skill in the art to form an Si epitaxial wafer doped with boron (or antimony or arsenic) at a temperature of 1000°C or higher on an Si substrate having an oxygen concentration of 4×10^{17} to 10×10^{17}, and then heat treating the wafer at a temperature from 450°C to 750°C, because it is suggested by Wijaranakula, in light of Wolf.

Still further, the final Office Action asserts that it would have been obvious to one of ordinary skill in the art to optimize the process parameters, including temperature, such that oxygen precipitation nuclei were formed (thus increasing the bulk defect density) and not reducing the needed and well know use of the bulk Si oxygen precipitates for gettering purposes because Wolf discloses such use for oxygen precipitates in the bulk of Si wafers and temperatures for annealing such wafers.

There final office Action failed to provide any motivation to combine Wijaranakula and Wolf to arrive at the claimed invention

According to M.P.E.P. § 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to arrive at the claimed invention where there is **some teaching, suggestion, or motivation** to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Additionally, the mere fact that the prior art may be combined or modified does not render the resultant combination obvious, unless the prior art suggests the desirability of the combination.

Thus, the Appellant submits that the rejection is based upon impermissible hindsight reconstruction because the only reason for modifying Wijaranakula in the manner suggested was gleaned from Appellant's own disclosure. The final Office

Action failed to proffer any motivation as to why one of ordinary skill in the art would be compelled to modify the references.

The oxygen concentration range and the epitaxial wafer heat treatment range are not merely optimized process parameters

Appellant's disclosure for example, at page 4, discusses that unless the interstitial oxygen concentration is in a range of 4×10^{17} and preferably 6×10^{17} atoms/cm^3, it is hard to form an oxygen concentration precipitation nucleus. If the interstitial oxygen concentration exceeds 10×10^{17} atoms/cm^3, too many oxygen precipitation nuclei are formed, which increases the possibility of wafer deformation. Therefore, Appellant's specification clearly demonstrates that these features have a specific purpose and are not mere design choices.

Further, Wijaranakula at column 5, lines 33-66, in process step 48, discloses that after the epitaxial layer is deposited, the wafer is annealed at a temperature of 600° - 900° C, and in process step 50, the wafer is heated at a temperature between 850°-1200° C. However, Appellant's disclosure for example, at page 7, discusses that when the epitaxial layer is grown on the silicon wafer at temperatures of 1000° or higher, many of the oxygen precipitation nuclei are dissolved into solid solution to reduce the number of oxygen precipitation nuclei. Further, on page 8 of Appellant's disclosure for example, it is stated that when the wafer is heated at a temperature of 450°-750° C, the bulk defect density rises. Therefore, Appellant's specification clearly demonstrates that these claimed features also have a specific purpose and are not mere design choices.

Wijaranakula or Wolf, either alone or in combination, fail to disclose or suggest a process for manufacturing a silicon epitaxial wafer including the steps of forming an

epitaxial layer on a silicon substrate with an interstitial oxygen concentration in a range of from 4 x $10^{17}/cm^3$ to 10 x $10^{17}/cm^3$ at a temperature of 1000° C or higher to obtain a silicon epitaxial wafer, as recited in claim 6. Wijaranakula or Wolf, either alone or in combination, also fail to disclose or suggest the steps of applying heat treatment to the silicon epitaxial wafer at a temperature in a range of from 450° C to 750° C, thereby forming new oxygen precipitation nuclei and increasing the bulk defect density, without reducing internal gettering, as recited in claim 6.

There is no disclosure or suggestion in Wijaranakula, as modified by Wolf, to vary the substrate resistivity of the epitaxial wafer

The final Office Action further asserts that it would have been obvious to one of ordinary skill in the art at the time of the invention that the resistivity of such a wafer would include a range of 0.02 ohm-cm or lower because such is disclosed by Wolf on page 26, as known to be a function of doping concentration.

An object of the present invention is to provide a novel manufacturing process for an epitaxial wafer having internal gettering ability. Claims 10-13 further recite that the substrate resistivity of the epitaxial layer is 0.02 Ω-cm or lower. This substrate resistivity is preferable in order to attain the desired effect of the present invention. Fig. 2 of the present invention shows the relationship between the heat treatment temperature and the bulk density after epitaxial growth. The bulk density rises depending on the temperature. As discussed in Appellant's specification, the lower the resistivity, the higher the effect of the heat treatment. Fig. 2 shows that when using a P-type silicon substrate with a resistivity 0.016 Ω-cm and 0.008 Ω-cm, the bulk defect density is much

higher than that with a 10 Ω-cm resistivity, after performing the heat treatment at a temperature between 450°C and 750°C. Additionally, it is known that when using an N-type silicon substrate with 0.02 Ω-cm or lower, oxygen is hard to be precipitated therein. However, according to the present invention, even if using an N-type silicon substrate, the bulk defect density can be increased.

Wolf, by contrast, only teaches the range of resistivity which can be used to manufacture a mere normal silicon wafer. Wolf is silent on increasing the bulk defect density of an epitaxial wafer or producing an epitaxial wafer having remarkable internal gettering ability, which are benefits of the claimed invention.

The epitaxial wafer of Wijaranakula is useful as a calibration wafer for measurement of thickness of a microdefect-free layer (Abstract), while an epitaxial wafer of the present invention is for a device fabrication process. As a result, the epitaxial wafer of Wijaranakula includes a bulk region having large, uniformly distributed oxide microdefects (see column 3, lines 39-42). Furthermore, Wijaranakula teaches after growing an epitaxial layer, the semiconductor silicon substrate is annealed at a temperature preferably between 600°C and 900°C for longer than 24 hours, preferably between 48 and 72 hours (see column 5, lines 33-38). On the other hand, since the epitaxial wafer of the present invention is for a device fabrication process, in view of productivity, the heat treatment time is within 24 hours, which is also a benefit of the claimed configuration.

Thus, Wijaranakula or Wolf, either alone or in combination, fail to disclose or suggest that the substrate resistivity of the epitaxial layer should be 0.02 Ω-cm or lower, as recited in claims 10-13.

In sum, Wijaranakula, as modified by Wolf, fails to disclose or suggest the claimed invention. Therefore, assuming *arguendo* that the references can be combined as suggested, the combination would still fail to result in the claimed invention.

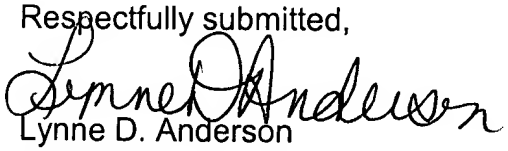
Still further, because claims 7-21 are dependent on claim 6, Appellant submits that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art, for at least the reasons set forth above with respect to claim 6.

For all of the above noted reasons, it is strongly contended that certain clear differences exist between the present invention as claimed in claims 6-21 and the prior art relied upon by the Examiner.

This final rejection being in error, therefore, it is respectfully requested that this honorable Board of Patent Appeals and Interferences reverse the Examiner's decision in this case and indicate the allowability of application claims 6-21.

In the event that this paper is not being timely filed, the Appellant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees which may be due with respect to this paper may be charged to our Deposit Account No. 01-2300, referencing docket number 107242-00024.

Respectfully submitted,



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APPENDIX 1

CLAIMS ON APPEAL

1. - 5. (Cancelled)

6. (Previously Presented) A manufacturing process for a silicon epitaxial wafer comprising the steps of:

forming an epitaxial layer on a silicon substrate with an interstitial oxygen concentration in a range of from $4 \times 10^{17}/cm^3$ to $10 \times 10^{17}/cm^3$ at a temperature of 1000° C or higher to obtain a silicon epitaxial wafer; and

applying heat treatment to the silicon epitaxial wafer at a temperature in a range of from 450° C to 750° C;

thereby forming new oxygen precipitation nuclei and increasing bulk defect density, without reducing internal gettering.

7. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 6, wherein the interstitial oxygen concentration is in a range of from $6 \times 10^{17}/cm^3$ to $10 \times 10^{17}/cm^3$.

8. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 6, wherein the heat treatment temperature is in a range of from 500° C to 700° C.

9. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 7, wherein the heat treatment temperature is in a range of from 500° C to 700° C.

10. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 6, wherein a substrate resistivity of the epitaxial wafer is 0.02 Ω-cm or lower.

11. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 7, wherein a substrate resistivity of the epitaxial wafer is 0.02 Ω-cm or lower.

12. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 8, wherein a substrate resistivity of the epitaxial wafer is 0.02 Ω-cm or lower.

13. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 9, wherein a substrate resistivity of the epitaxial wafer is 0.02 Ω-cm or lower.

14. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 6, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

15. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 7, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

16. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 8, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

17. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 9, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

18. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 10, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

19. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 11, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

20. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 12, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

21. (Previously Presented) The manufacturing process for a silicon epitaxial wafer according to claim 13, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.